9, 2001. In view of the claims as amended and the following remarks, it is submitted that the application is now in the condition for allowance.

Claims 56,57,58,60,67,68,69 and 71 were rejected under 35 U.S.C. § 112, second paragraph because of the word "same." That word was removed and the claims were rewritten to overcome the rejection.

Claims 52-58, 62, 65-69 and 73 were rejected unde4 35 U.S.C. §102(b) as being anticipated by Pruniaux et al. (3,823,352).

The claimed process is for a planar device, not a mesa device. The steps of claims 52 and 65 are amended to distinguish the inventive planar process from the mesa process of Puniaux. The reference fails to show or suggest forming well and source regions in the first surface and forming gate regions between the well and source regions. The amendment is supported by the wells 56, 76, the sources 22, 57, 77 and the gates 54, 55 and 74, 75.

Pruniaux also fails to teach that its drain contact 16 lowers resistance. As such, the rejection is premised upon an unstated finding that the drain contact 16 inherently lowers resistance. Pruniaux only teaches that the massive contact 16 improves thermal characteristics. Col. 3, lines 62,63. Pruniaux is silent on whether the contact reduces resistivity.

The invention defined by claims 53-58, 62, 65-59 and 73 is distinguished from Pruniaux for the same reasons as claim 52. Claims 57 and 68 are further distinguished from Pruniaux by the recitation of a lower limit of "not less than about 0.4 percent." Prunaiux fails to show or suggest that limit. Claims 59, 60, 70 and 71 are distinguished from Prunaiux because it fails to show or suggest an array of recesses, in particular a grid array of recesses. The drain contact/heat sink 16 is a single contact. It is not an array. Prunaiux fails to show more than one drain contact/heat sink under its device.

Claims 52-57, 59-63, 65-68 and 70-74 were rejected under 35 U.S.C. §102(b) as being anticipated by Okabe, et al. (U. S. Patent No. 5,663,096).

Okabe fails to show the invention as set forth in claim 52. That invention calls for recesses in the second surface of the substrate and for resistivity lowering bodies in those recesses. There are no recesses in Okabe.

It appears the rejection relies upon the rough surface 22 as a basis for finding

recesses in Okabe. Applicant submits that the surface 22 is simply that, a rough surface and does not include recesses as set forth in the claims.

The drawings in Okabe show a rough surface to indicate that the lower surface of the wafer is rough after it has been thinned by an abrasive removal process. Okabe teaches the use of a grindstone 18 as shown in Fig. 3 for removing material from the back surface. Okabe nowhere uses the term "recess" in his disclosure.

Applicant submits that the Examiner, as one skilled in the art, will recognize the difference between recesses that are intentionally formed in a surface and a randomly roughened surface that results from an abrasive operation.

In order to positively distinguish from Okabe, claims 52 and 65 have a step of removing material from the lower surface of the wafer. That step may be made at any time during the process and is preferably made prior to the formation of the recesses. Claims 52 and 65 positively distinguish between a removal step and a recess formation step and are patentable over Okabe because Okabe fails to show a recess formation step.

Because Okabe does not form recesses, it is not available as a reference against the remaining dependent claims 53-64 and 66-75. Accordingly, those claims are likewise distinguished over the Okabe patent for the reasons given above.

Claims 65-75 are also distinguished from Okabe on grounds that Okabe does not show resistivity lowering bodies extending from the second surface of the substrate. As pointed out above, there are no recesses in Okabe and thus, the ohmic electrode 26 is necessarily formed only on the surface 22.

Applicant traverses the rejection of claims 56 and 67. The rejection there is based upon the assumption that Okabe discloses a resistivity lowering body of platinum, gold or silver. That is incorrect. A review of the disclosure of Okabe finds no mention of platinum or silver. Likewise, the only mention of gold in Okabe is for the outermost or top layer on the back substrate. That top layer is not a resistive body and certainly is not below the surface of the substrate.

Applicant traverses the rejection of claims 57 and 68. For the same reasons given above, Okabe does not show or suggest resistivity-lowering bodies. Instead, the Okabe structure would likely generate a graph similar to the diamond graph shown in Figs. 7-14.

Applicant traverses the rejection of claims 59-61 and 70-72. The rotational

lapping operation performed Okabe does not generate a grid pattern. A grid by definition includes parallel lines. Okabe fails to show or suggest any grid pattern of parallel lines. Indeed, the Examiner, as one skilled in the art, knows that a rotating abrasive grinding tool applied to a surface does not produce trenches or parallel features. In this regard, Applicant points out that Okabe never identifies any trenches or recesses in their patent. Instead, reference number 22 is directed to a ground surface.

Claims 63, 64, 74, and 75 are rejected under 35 U.S.C. § 103(a) as obvious based on Pruniaux. They are rejected based on a combination of Pruniaux and Okabe who mentions usisng its process to form an IGBT. As explained above, Pruniaux fails to show or suggest the planar devices formed by the process. Hence, even is an IGBT were formed with the Pruinaux process, that process would not follow the claimed steps that require surface wells and surface source regions separated by gates.

The claims as amended distinguish themselves from the applied art of record. As such, the invention is patentable and a notice of allowance is requested.

Respectfully submitted,

Thomas R. FitzGerald
Registration No. 26,730

JAECKLE FLEISCHMANN & MUGEL, LLP
39 State Street, Suite 200
Rochester, New York 14614-1310
Tel. (716) 262-3640
Fax: (716) 262-4133

Certificate of Mailing - 37 CFR 1.8(a)

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Assistant Commissioner for Patents, Washington, D.C. 20231, on the date below.

12-10-01
Date

ADDENDUM WITH MARKED UP CLAIMS AS AMENDED

This addendum shows all claims currently in the application. Only that claims that have been amended are indicated as "amended."

52. (amended) [A method for making a semiconductor device comprising a semiconductor substrate having a lowered effective electrical resistivity, the method comprising:

forming at least one device active region in the semiconductor substrate adjacent a first surface thereof;

forming at least one recess extending from a second surface of the substrate, opposite the first surface, into interior portions of the semiconductor substrate; and forming at least one resistivity-lowering body in the least one recess of the semiconductor substrate, the at least one resistivity-lowering body comprising a material having an electrical resistivity lower than an electrical resistivity of the semiconductor substrate.]

A method for making a semiconductor device comprising a semiconductor substrate having a lowered effective electrical resistivity, the method comprising:

in a first surface, forming one or more well regions comprising dopants of one polarity;

in the first surface and in said body regions, forming source regions of dopants of an opposite polarity, the source regions laterally spaced from each other;

forming gate regions between the laterally spaced source regions;

in a second surface opposite the first surface, forming a layer of dopants;

removing material from the second surface to reduce the thickness of said substrate;

forming one or more recesses extending from the second surface of the substrate into interior portions of the semiconductor substrate; and

forming a resistivity-lowering body in one or more of the recesses, the resistivity-lowering bodies comprising a material having an electrical resistivity lower than an electrical resistivity of the semiconductor substrate.

53. A method according to Claim 52 further comprising forming an electrical contact layer on the second surface of the semiconductor substrate being electrically connected to the

at least one resistivity-lowering body.

54. A method according to Claim 52 wherein forming the at least one resistivity-lowering body comprises filling an associated recess.

55.(amended) A method according to Claim 52 further comprising forming a barrier layer lining [the] at least one recess.

56.(amended) A method according to Claim 52 wherein forming the [at least one] resistivity-lowering body comprises forming [same] <u>said body</u> using an electrical conductor having an electrical resistivity less than about 10^{-4} Ω•cm.

57.(amended) A method according to Claim 52 wherein forming the [at least one] recesses and associated resistivity-lowering body comprises forming <u>the recesses and the assoicated resistivity lowering bodies</u> [same] to define a proportion of the semiconductor substrate area adjacent the at least one device active region <u>no less than</u> [greater] than about 0.4 percent.

58. A method according to Claim 52 wherein forming the [at least one] recesses and associated resistivity-lowering body comprises forming [same] <u>the recesses and the associated resistivity lowering bodies</u> to extend into the semiconductor substrate a distance greater than about 25 percent of a thickness of the semiconductor substrate.

59. A method according to Claim 52 wherein forming the at least one recess and associated resistivity-lowering body comprises forming an array of recesses and associated resistivity-lowering bodies.

60.(amended)

A method according to Claim 59 wherein forming the array of recesses and associated resistivity-lowering bodies comprises [forming same to be] <u>are</u> arranged in a grid pattern.

61. A method according to Claim 60 wherein forming the grid pattern comprises cutting

trenches in the second surface of the semiconductor substrate.

62. A method according to Claim 52 wherein forming the at least one device active region comprises forming at least one device active region for a metal-oxide semiconductor field-effect transistor (MOSFET).

63. A method according to Claim 52 wherein forming the at least one device active region comprises forming at least one device active region for an insulated gate bipolar transistor (IGBT).

64. A method according to Claim 52 wherein forming the at least one device active region comprises forming at least one active region of a microprocessor.

65.(amended) [A method for making a semiconductor device comprising a semiconductor substrate having a lowered effective electrical resistivity, the method comprising:

forming at least one device active region in the semiconductor substrate adjacent a first surface thereof; and forming at least one resistivity-lowering body extending from a second surface of the substrate, opposite the first surface, into interior portions of the semiconductor substrate, the at least one resistivity-lowering body comprising a material different than the semiconductor substrate and having an electrical resistivity lower than an electrical resistivity of the semiconductor substrate.]

A method for making a semiconductor device comprising a semiconductor substrate having a lowered effective electrical resistivity, the method comprising:

in a first surface, forming one or more well regions comprising dopants of one polarity;

in the first surface and in said body regions, forming source regions of dopants of an opposite polarity, the source regions laterally spaced from each other;

forming gate regions between the laterally spaced source regions;

in a second surface opposite the first surface, forming a layer of dopants;

removing material from the second surface to reduce the thickness of said substrate;

and forming one or more resistivity-lowering bodies extending from the second surface of the substrate into interior portions of the semiconductor substrate, the resistivity-lowering bodies comprising a material different than the semiconductor substrate and having an electrical resistivity lower than an electrical resistivity of the semiconductor substrate.

66. A method according to Claim 65 further comprising forming an electrical contact layer on the second surface of the semiconductor substrate being electrically connected to the at least one resistivity-lowering body.

67.(amended)

A method according to Claim 65 wherein [forming] the at least one resistivity-lowering body comprises [forming same using] an electrical conductor having an electrical resistivity less than about 10^{-4} Ω•cm.

68.(amended) A method according to Claim 65 wherein [forming] the [at least one] resistivity-lowering body comprises forming the resistivity-lowering body [same] to define a proportion of the semiconductor substrate area adjacent the at least one device active region not less than [greater] than about 0.4 percent.

69.(amended) A method according to Claim 65 wherein [forming] the [at least one] resistivity-lowering body [comprises forming same to] extends into the semiconductor substrate a distance greater than about 25 percent of a thickness of the semiconductor substrate.

70. A method according to Claim 65 wherein forming the at least one resistivity-lowering body comprises forming an array of resistivity-lowering bodies.

71.(amended) A method according to Claim 70 wherein [forming] the array of resistivity-lowering bodies comprises [forming same to be arranged in] a grid pattern.

72. A method according to Claim 71 wherein forming the grid pattern comprises cutting trenches in the second surface of the semiconductor substrate.

73. A method according to Claim 65 wherein forming the at least one device active region comprises forming at
least one device active region for a metal-oxide semiconductor field-effect transistor (MOSFET).

74. A method according to Claim 65 wherein forming the at least one device active region comprises forming at least one device active region for an insulated gate bipolar transistor (IGBT).

75. A method according to Claim 65 wherein forming the at least one device active region comprises forming at least one active region of a microprocessor.